

TSN-SW | ETHERNET TSN SWITCH IP CORE

Time-Sensitive Networking (TSN) is a set of sub-standards that enhance the existing Ethernet specification towards time synchronization and deterministic communication in switched networks according to existing IEEE 802.1 and 802.3 standards. The goal is it to make Ethernet more suitable for the advancing needs of industrial, automotive and other applications. The TSN-SW is suitable for multiport switches with or without integrated endpoint functionality. A configurable number of 2 to 24 full-duplex Ethernet ports plus one internal port are available. The design implements a 1GbE switching bar with cut-through capability at wire speed. It provides time-sensitive networking for full-duplex point-to-point Ethernet communication.

Several hundreds of customers worldwide have relied on the quality of Fraunhofer IPMS IP-Core solutions for FPGA and ASIC designs and the comprehensive technical support for over 20 years.

Applications

The TSN-SW IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks. The TSN-SW IP can be utilized for embedding real-time TSN applications into regular Ethernet networks. It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Featuring a configurable number of ports, the Layer-2 switch operates in cut-through mode at wire speed and can provide sub-microsecond port-to-port latency. The core is hence suitable for applications with demanding real-time requirements.

Verification

Interoperability of sub-modules is constantly tested within TSN plug-fests by LNI4.0 and Industrial Internet Consortium (IIC).



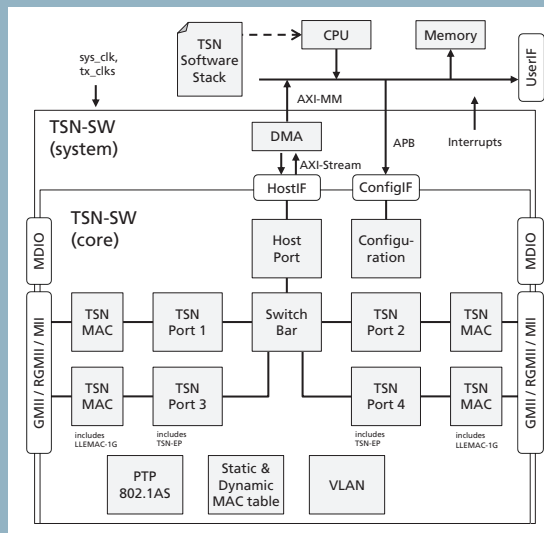
Contact

Monika Beck
+49 351 88 23 - 274
monika.beck@ipms.fraunhofer.de

Dr. Frank Deicke
+49 351 88 23 - 385
frank.deicke@ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Str. 2
01109 Dresden
Germany

www.ipms.fraunhofer.de



Schematic diagram of the TSN-SW IP Core.

TSN Features

- Time synchronisation (IEEE 802.1 AS-2020)
- Traffic-Shaping (IEEE 802.1 Qav and Qbv)
- Frame Preemption (IEEE 802.3br and IEEE 802.1Qbu)
- Frame Replication and Elimination (IEEE 802.1CB)
- SRP Enhancements (IEEE 802.1Qcc)
- Stream Filtering and Policing (IEEE 802.1Qci)
- Ethernet MAC communication (IEEE 802.3)
- 802.1Q Tagged VLAN support
- Configurable VLAN-PCP to TSN-Queue Mapping (QoS by PCP)
- IPMS AXI4-DMA core optional

Easy Integration

- Platform independent implementation into any FPGA or foundry technology
- TSN-SW IP core can be attached to custom SoC or a complete TSN-SW can be provided
- Intel Altera based evaluation platform
- Xilinx based evaluation platform
- Set of demo projects for Xilinx and Intel Altera
- Configurable feature set
- Responsive support
- TSN Evaluation Kit available

IEEE 802.1Q Switch Features

- Low-latency Layer 2 switch cut-through switching at wire speed
- Configurable number of 2 to 24 full-duplex Ethernet ports plus one internal port
- Supports up to 1024 dynamic and static MAC table entries
- 8 Gbps Fwd-Bandwidth at 4 Ports
- Cut-through or store-and-forward TSN frame forwarding
- Ports run full-duplex at 10/100/1000 Ethernet
- PHY configuration via MDIO
- Port based 12bit VLAN-ID support
- Automatic ageing table support
- Statistics by widely configurable counters

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- TSN FreeRTOS Unified Framework, CLI example, PTP-AS2020
- FreeRTOS example projects
- Linux driver reference design

Designed for Usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- 2.5/5/10+ Gbps on request
- Host Interfaces to AXI, AvalonST/MM
- PHY Interfaces to MII, GMII and RGMII
- Memory-Mapped MDIO interface per port for PHY configuration

Data Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 32 bit AXI-Streams for TX data
- Avalon interfaces available
- More interfaces upon request



TSN Evaluation Kit:
Xilinx ZCU102 or Intel Netleap (Cyclone V SoC); implemented IPMS TSN-IP core for switch applications (TSN-SW).

TSN-EP | ETHERNET TSN ENDPOINT CORE

Time-Sensitive Networking (TSN) enhances the Ethernet specification towards time synchronization and deterministic communication (specifically IEEE 802.1 and 802.3). The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications. The TSN Ethernet IP core TSN-EP eases the integration of devices into networks complying with the TSN standards. It provides time-sensitive networking for full duplex point-to-point Ethernet communication. The IP core consists of three sub-modules for time synchronization, traffic shaping and low latency Ethernet MAC communication.

Several hundred of customers worldwide have relied on the quality of Fraunhofer IPMS IP-Core solutions for FPGA and ASIC designs and the comprehensive technical support for over 20 years.

Applications

The TSN-EP IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks requiring time synchronization as well as robust, low-latency, and deterministic communication.

It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Verification

Interoperability of sub-modules is constantly tested within TSN plug-fests by LNI 4.0 and Industrial Internet Consortium (IIC).



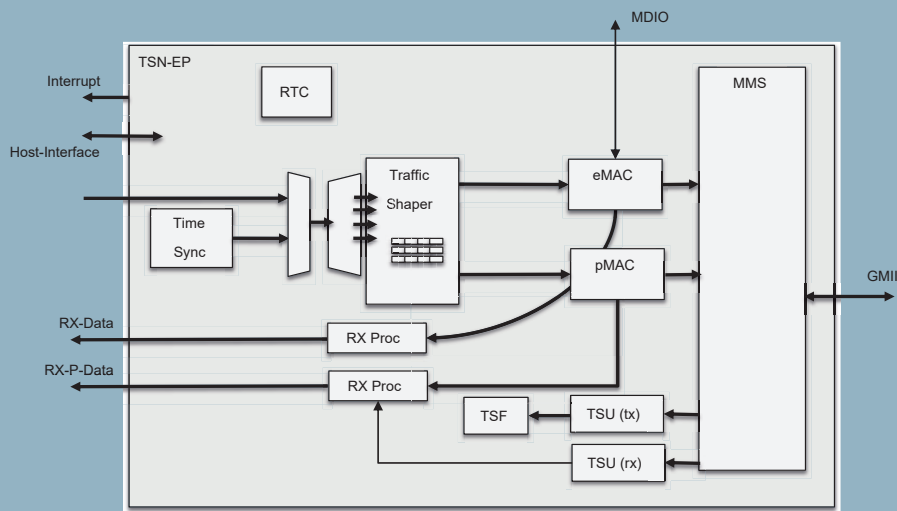
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Schematic diagram of the TSN-EP.

TSN Features

- Time synchronisation (IEEE 802.1 AS-2020)
- Traffic-Shaping (IEEE 802.1 Qav and Qbv)
- Frame Preemption (IEEE 802.3br and IEEE 802.1Qbu)
- Frame Replication and Elimination (IEEE 802.1CB)
- SRP Enhancements (IEEE 802.1Qcc)
- Stream Filtering and Policing (IEEE 802.1Qci)
- Ethernet MAC communication (IEEE 802.3)
- IPMS AXI4-DMA core optional

Easy Integration

- Platform independent implementation into any FPGA or foundry technology
- Intel & Xilinx based evaluation platforms
- Set of demo projects for Xilinx and Altera
- ASIC & FPGA design support

Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 – 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- PHY: MII, GMII, RGMII

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- TSN FreeRTOS Unified Framework, CLI example, PTP-AS2020
- FreeRTOS example projects
- Linux driver reference design
- TSN network configuration examples

Designed for Usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- 2.5/5/10+ Gbps on request



TSN Evaluation Kit: Xilinx ZCU102 or Intel Netleap (Cyclone V SoC); implemented IPMS TSN-IP core for endpoint applications (TSN-EP).

TSN-SE | ETHERNET TSN SWITCHED ENDPOINT CORE

Time-Sensitive Networking (TSN) is a set of sub-standards that enhance the existing Ethernet specification towards time synchronization and deterministic communication in switched networks according to existing IEEE 802.1 and 802.3 standards. The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications. The TSN Ethernet IP core TSN-SE provides TSN switched endpoint functionality and eases the integration of devices into networks complying with the TSN standards. Two external 10/100/1000 Mbits/s ports are available beside an internal CPU port. The design implements a 1 GbE switching bar with cut-through capability. It provides time-sensitive networking for full-duplex point-to-point Ethernet communication enabling daisy chaining, devices, ring architectures or physical redundant communication. The IP core consists of two instances of the TSN-EP IP and a switching bar as well as additional routing logic optimized for low latency communication.

Several hundreds of customers worldwide have relied on the quality of Fraunhofer IPMS IP-Core solutions for FPGA and ASIC designs and the comprehensive technical support for over 20 years.

Applications

The TSN-SE IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks. The TSN-SE IP can be utilized for embedding real-time TSN applications into regular Ethernet networks. It is suitable for daisy-chained networks such as rings.

It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Verification

Interoperability of sub-modules is constantly tested within TSN plug-fests by LNI4.0 and Industrial Internet Consortium (IIC).



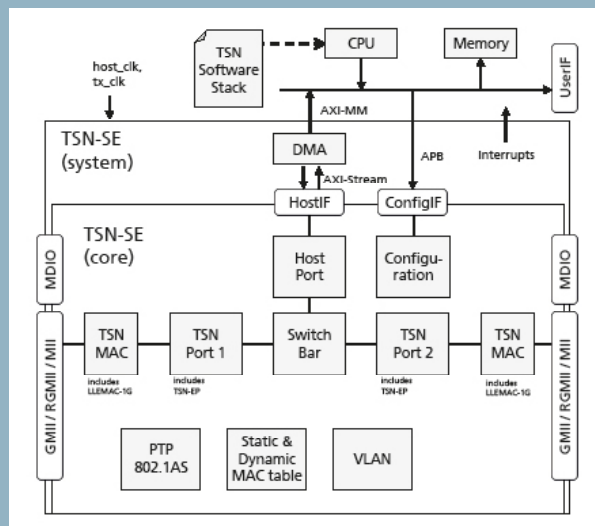
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Photonic Microsystems IPMS
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Schematic diagram of the TSN-SE IP Core.

TSN Features

- Time synchronisation (IEEE 802.1 AS-2020)
- Traffic-Shaping (IEEE 802.1 Qav and Qbv)
- Frame Preemption (IEEE 802.3br and IEEE 802.1Qbu)
- Frame Replication and Elimination (IEEE 802.1CB)
- SRP Enhancements (IEEE 802.1Qcc)
- Stream Filtering and Policing (IEEE 802.1Qci)
- Ethernet MAC communication (IEEE 802.3)
- IPMS AXI4-DMA core optional

Easy Integration

- Platform independent implementation into any FPGA or foundry technology
- TSN-SE IP core can be attached to custom SoC, or a complete TSN-SE can be provided
- Intel & Xilinx based evaluation platforms
- Set of demo projects for Xilinx and Altera
- Configurable feature set
- Responsive support
- TSN Evaluation Kit available

IEEE 802.1Q Switch Features

- Layer 2 switch cut-through architecture
- 2 Gigabit TSN ports and 1 host port
- Supports up to 1024 dynamic and 1024 static MAC table entries
- Supports IEEE 802.1Q VLAN-tags with up to 1024 entries
- Ports run full-duplex at 10/100/1000 Ethernet
- PHY configuration via MDIO

TSN Evaluation Xilinx ZCU102 or Intel Netleap (Cyclone V SoC); implemented IPMS TSN-IP core for switched endpoint applications (TSN-SE).

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- TSN FreeRTOS Unified Framework, CLI example, PTP-AS2020
- FreeRTOS example projects
- Linux driver reference design

Designed for Usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- 2.5/5/10+ Gbps on request
- PHY Interfaces to MII, GMII and RGMII
- Ingress latency: 6 Rx clock cycles
- Egress latency: 10 Tx clock cycles

Data Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 – 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- More interfaces upon request

